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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/771,630	COL, GERARD M.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-21* is/are allowed.

6)☒ Claim(s) *1-16 and 22-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 15,16,22-27,32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 15 (line 5) contains the language "computer readable code causes the microprocessor". It is unclear what operation is occurring (is the computer code somehow creating a microprocessor or something else).

4. Claim 16 (lines 3-4) contains the language "computer-readable program code provides the microprocessor". It is unclear what operation is occurring (is the computer readable program code somehow creating or obtaining a microprocessor or something else.

5. Claim 32 (lines 3-4) contain the language computer readable code for providing a pipeline microprocessor and in claim 32 (lines 8-9) contain "program code for providing an address stage" and claim 32 (lines 16-17)'program code for providing an early register file. It is unclear what operation is occurring (is the program code somehow creating or obtaining a microprocessor and address stage and early register file or something else.

6. Claim 22 contains the language "generate a selectively valid result". The meaning of this language is unclear. (i.e., does the system select a valid result from

results or does the system select whether the result will be seen as valid or something else). Also claim 22, contains stalling when an instruction specifies memory address generation and not stalling when the instruction specifies result generation. Generating an address comprises producing an resultant address or result. Therefore it is unclear if the operations that cause the stall and the operation that cause the not stall operation is the same operation or not. Claims 23-27 depend on claim 22 and are rejected for the same reasons claim 22 is rejected.

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 15,16, 32 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claims respectively contain the following language "computer-readable program code provides the microprocessor"(claim 15, lines 3-4). "computer readable code for providing a pipeline microprocessor"(claim 16(lines 3-4) and contain "program code for providing an address stage(claim 32, lines 3-4) and 'program code for providing an early register file(claim 32, lines 8-9). These operations of providing hardware elements using abstract program code has not been described in a manner so one of ordinary skill would be able to perform these

operations. What physical elements are used to fabricate or retrieve the elements of the hardware devices? And how does the program code interact with the physical elements to create or obtain the hardware elements?

Claim Rejections - 35 USC § 101

9. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

10. Claims 15,16,32 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

11. Claim 15 is directed to a computer program product comprising a computer usable medium having a computer readable code causes the microprocessor. The computer program product is not within any of the statutory categories of invention (machine, manufacture, composition of memory or process). The computer usable medium is disclosed in one embodiment as a computer readable transmission medium with the example given being a carrier wave (see page 44 of the specification of the instant application). A carrier wave is not within any of the statutory categories of invention. Also the carrier wave is not tangibly embodied in a manner to so as to be executable. Similarly claim 16 is directed to a signal embodied in a transmission medium comprising computer readable program code. The signal embodied in a transmission medium is not within one of the statutory classes of invention and also is not tangibly embodied in a manner so as to be executable (the claim consists of intangible media). Also claim 32 is directed to a data signal embodied in a transmission medium the comprises computer readable program code. The code consists of merely

portions of a data signal. This data signal is not one of the statutory classes of invention (machine, manufacture, composition of matter or process). Further this signal is not tangibly embodied so as to be executable.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1-14,28, and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Henry (patent No. 5,812,813).

14. Henry taught the invention as claimed including a data processing ("DP") system comprising: a pipeline microprocessor having a architected register file (517)(e.g., see fig. 5 and col. 11, lines 19-22) and at least one final execution unit (236) for generating final results of instructions (e.g., see fig. 2,) comprising:

a) Address stage (ADDRESS (A)) located earlier in the pipeline than a stage in which the final execution unit (236) is located, including an early execution unit (228) configured to generate early results of instructions prior to generation the final results of the instructions by the final execution unit (e.g., see col. 5, lines 1-64); an early register file (temporary registers 222, 224, 226, 232, 234, e.g., see col. 6, lines 37-48) coupled to said early execution unit corresponding to the architected register file configured to store said early result and to provide said early results to said early execution unit for

generating early results of subsequent instructions (e.g., see fig. 2 and col. 5, lines 1-64 and col. 6, lines 1-8) wherein the architected register file(218) is updated only with the final results and not with said early results (e.g., see col. 5, line 65-col. 6, line 8 and col. 6, lines 37-65).

15. As per claim 2,3,4,5 Henry taught the early execution unit is configured to execute only a subset of instructions of the microprocessor wherein the subset of instructions executable by the early execution unit (address unit) includes shift, Boolean and arithmetic instructions (e.g., see col. 5,lines 42-52).[the address unit includes an arithmetic logic unit where a arithmetic logic unit would have been inherently able to perform arithmetic operations, and/or logical operations, and/or shift operations).

16. As to the limitations of claim 6,7 Henry taught a bus that provides for the generation of early results in response to separate instructions in successive clock cycles (e.g., see figs. 2, 4) [e.g., POP IP immediately precedes POP CS and the results for each of theses instructions are generated in successive clock cycles in fig. 4].

17. As per claim 8, Henry taught a result write-back stage located later in the pipeline that a stage in which the final execution is located, configured to update the architected register file with the final results generated by the final generation unit wherein only the early register is updated with early results (e.g., see figs. 2, 4) (e.g., see col. 5, line 65-col. 6, line 8 and col. 6, lines 37-65).

18. As per claim 9, Henry taught the early execution logic is configured to generate memory address using early results received ad operand from the early register file (e.g., see col. 5, line 42-col. 6, line 8 and col. 6, lines 37-65).

19. As per claim 10,14 Henry taught the early execution unit as a single pipeline stage that is configured to generate memory addresses for stack memory locations and to generate memory address for non-stack memory locations (e.g., see col. 7, lines 56-col. 8, line 3 and col. 5, lines 42-51).

20. As per claim 11, Henry taught the results in the early register file may or may not be valid (e.g., see col. 11, lines 17-29)[the system indicates whether a temporary register is modified which would have been equivalent to determining if the data in the register was valid].

21. As per claim 12,13, Henry taught the microprocessor was a scalar processor (e.g., see col. 5, lines 52-64) and microprocessor issues instructions in program order (e.g., see col. 7,line 11-col. 8, lines 64 and figs. 2,3,4).

22. As per claim 28, Henry taught generating a first result of a first instruction in an address stage of the pipeline, wherein the first result is potentially invalid(e.g,. see col. 6, lines 49-67and col. 11,lines 17-29); storing the first result into an early register file of the microprocessor(e.g., see col. 7, lines 27-55); generating a second result of a second instruction in the address stage using the first result from the early register file as an input operand to the second instruction (col. 7, line 56-col. 8, line 3); storing the second result into the early register file(col. 8, lines 4-16); and generating a memory address for a third instruction using the second result from the early register file as an input operand to the third instruction(e.g., see col.8, lines 17-49 and fig. 4).

23. As per claim 29, Henry taught accumulating status flags (e.g., see col. 9, line 65-col. 10, line 21).

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
> Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over

25. Claims 15,16, 30,31,32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Henry (patent No. 5,812,813).

26. Henry taught the invention substantially as claimed including a data processing ("DP") system comprising (as per claims 1 as it pertains to claims to claims 15,16), and 15,16,32): a pipeline microprocessor having a architected register file (517)(e.g., see fig. 5 and col. 11, lines 19-22) and at least one final execution unit (236) for generating final results of instructions (e.g., see fig. 2,) comprising:

Address stage (ADDRESS (A)) located earlier in the pipeline than a stage in which the final execution unit (236) is located, including an early execution unit (228) configured to generate early results of instructions prior to generation the final results of the instructions by the final execution unit (e.g., see col. 5, lines 1-64); an early register file (temporary registers 222, 224, 226, 232, 234, e.g., see col. 6, lines 37-48) coupled to said early execution unit corresponding to the architected register file configured to store said early result and to provide said early results to said early execution unit for generating early results of subsequent instructions (e.g., see fig. 2 and col. 5, lines 1-64 and col. 6, lines 1-8) wherein the architected register file(218) is updated only with the

final results and not with said early results (e.g., see col. 5, line 65-col. 6, line 8 and col. 6, lines 37-65). Henry taught the elements and operations of the claim as discussed above. However Henry did not expressly detail the elements and operation were a computer data signal comprising program code for providing the elements and operations. However as the claim is best understood the code for controlling elements to perform the claimed operations is in the form of a data signal comprising program code. Since the system of Henry is a data processing system it would have required instructions to control the system to perform the operations taught by Henry. Also it would have been within the level of skill of one of ordinary skill in that art at the time of the claimed invention to convert the program code to a signal for remote transmission. One of ordinary skill would have been motivated to convert the program code into a signal at least to distribute the program code for sale or for providing the microprocessor configuration to a remote location.

27. As per claim 28(as it pertains to claim 30), Henry taught generating a first result of a first instruction in an address stage of the pipeline, wherein the first result is potentially invalid (e.g., see col. 6, lines 49-67and col. 11,lines 17-29); storing the first result into an early register file of the microprocessor(e.g., see col. 7, lines 27-55); generating a second result of a second instruction in the address stage using the first result from the early register file as an input operand to the second instruction (col. 7, line 56-col. 8, line 3); storing the second result into the early register file(col. 8, lines 4-16); and generating a memory address for a third instruction using the second result from the early register file as an input operand to the third instruction(e.g., see col.8,

lines 17-49 and fig. 4).As per claim 29(as it pertains to claim 30), Henry taught accumulating status flags (e.g., see col. 9, line 65-col. 10, line 21). Henry did not expressly detail(claim 30) invalidating the early status flags if the second result is invalid. However Henry taught overwriting of the registers and allowing the exception handler to read temporary registers for the data in the original registers. Therefore it would have been obvious to one of ordinary skill that early status flags(in the embodiment that used flags instead of combinatorial logic) were invalidated or overwritten by succeeding instructions when the flag for a succeeding instruction was to indicate an invalid result (e.g., see col. 11, lines 17-37). Henry taught (claim 31) when the condition indicated that the conditional instruction was satisfied and the flags were valid then the operation in the Henry system was performed (e.g., see col. 10, lines 36-61).

Allowable Subject Matter

Claims 17-21are allowed.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Meier (patent No. 6,393,555) disclosed a rapid execution of FCMOV following FCOMI by storing comparison results in temporary register in floating point unit (e.g., see abstract).

Tran (patent No. 6,065,103) disclosed a speculative store buffer (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER